

<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/922,639	PARVATHALA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	CHAMELI C DAS	2122	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 3/12/05.
2. ☒ The allowed claim(s) is/are 2-12, 15-16, 18-26, 28-36 (newly numbered claims are 1-31).
3. ☒ The drawings filed on 27 September 2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |   |   |
|---|---|
| 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)                                 |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                | 6. <input checked="" type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date <u>3/16/05</u> . |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),<br>Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment   |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material          | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance                        |
|   | 9. <input type="checkbox"/> Other _____.  |

1. This action is in response to the final office action filed on 2/28/05.
2. Claims 1, 13-14, 17 and 27 have been canceled.
3. Claims 3, 8, 11, 12, 15, 19, 21, 24, 28, 29, 31 and 34 have been amended.
4. Claims 2-12, 15-16, 18-26 and 28-36 have been allowed.

#### **EXAMINER'S AMENDMENT**

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Dany J. Padys, applicant's attorney on 3/16/05.

The application has been amended as follows:

***In claims:***

***In claim 2 (Currently amended)***

at line 4, after "a", delete [SBE] and insert -- software built-in self-test engine (SBE) --.

***In claim 3 (Currently amended)***

at line 4, after "a", delete [SBE] and insert -- software built-in self-test engine (SBE) --.

***In claim 8 (Currently amended)***

at line 4, delete [an RIT] and insert -- a random instruction test (RIT) --

at line 5, delete [RIT generator] and insert --RIT-G--.

***In claim 11 (Currently amended)***

at line 4, after “a”, delete [SBE] and insert -- software built in self-test engine (SBE) --

at line 9, delete [an RIT generator] and insert -- a random instruction test generator (RIT-G) --

at line 9, delete [RIT] and insert -- random instruction test (RIT) --

***In claim 15 (Currently amended)***

at line 4, after “a”, delete [SBE] and insert -- software built-in self-test engine (SBE) --

at line 21, [(M)] should be replaced by --(“M”) --

at line 21, [ N and M ] should be replaced by -- “N” and “M”--.

***In claim 21 (Currently amended)***

at line 4, delete [an RIT] and insert -- a random instruction test (RIT) --

at line 5, delete [RIT generator] and insert --RIT-G--.

***In claim 24 (Currently amended)***

at line 11, delete [an RIT generator] and insert -- a random instruction test generator (RIT-G) --

at line 11, after “compact”, delete [RIT] and insert -- random instruction test (RIT) -- .

***In claim 25 (Currently amended)***

at line 12, [(M)] should be replaced by --("M") --

at line 12, [ N and M ] should be replaced by -- "N" and "M"--.

***In claim 31 (Currently amended)***

at line 4, delete [an RIT] and insert -- a random instruction test (RIT) --

at line 5, delete [an RIT generator] and insert -- a random instruction test generator (RIT-G) --.

***In claim 35 (Currently amended)***

at line 3, [(M)] should be replaced by --("M") --

at line 3, [ N and M ] should be replaced by -- "N" and "M"--.

***REASON FOR ALLOWANCE***

6. The following is an examiner's statement of reason for allowance:

The cited prior art taken alone or in combination fail to teach, in combination with the other claimed limitations, a system comprises a software built-in self-test engine (SBE) generation tool for generating a software built-in self-test engine (SBE), wherein said SBE generation tool comprises: a random instruction test generator (RIT-G) composer to receive the user directives and the instruction information and generate a compact RIT-G code; a code merger to merge code from the RIT-G composer, the test execution directive composer and the test result compaction module composer to generate the software built-in-self-test engine (SBE), as recited in the independent claims 2, 18 and 28.

The cited prior art taken alone or in combination fail to teach, in combination with the other claimed limitations, a system comprises a software built-in self-test engine (SBE) generation tool for generating a software built-in self-test engine (SBE), wherein said SBE is to be merged with an expected test result and then loaded on-board the complex device under test (DUT) so as to activate the re-generative functional test on the complex device under test (DUT) and make a comparison between test results of the re-generative functional test and the expected test result to check for design validation and/or manufacturing defects, as recited in the independent claims 3 and 29.

The cited prior art taken alone or in combination fail to teach, in combination with the other claimed limitations, a system comprising: a software built-in-self test engine (SBE) generation tool for generating a software built-in self-test engine (SBE), wherein said SBE comprises: a random instruction test generator (RIT-G) including random instruction test (RIT) machine code residing on-board the complex device under test (DUT) for generating the regenerated functional test; a test result compaction module including compression machine code to compress test results of the re-generated functional test for storage on-board the complex device under test (DUT), as recited in the independent claims 11 and 24.

The cited prior art taken alone or in combination fail to teach, in combination with the other claimed limitations, a system comprising: a software built-in self-test engine (SBE) generation tool for generating a software built-in self-test engine (SBE), wherein said SBE is programmed to generate and execute one or more ("N") instruction sequences, each sequence being executed on one or more ("M") data sets, where "N" and "M" represent an integer no less

than “1” and are user-specified numbers used in generating the SBE by the SBE generation tool, as recited in the independent claims 15 and 25.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

### ***Conclusion***

7. The prior art made or record and not relied upon is considered pertinent to applicant’s disclosure.

TITLE: Operating system debugger extensions for hypervisor debugging, US 6839892 B2

TITLE: Method and apparatus for making integrated circuits with built-in self-test, US 5572712

TITLE: Test system and manufacturing of semiconductor device, US 6400173 B1

TITLE: Deterministic random LBIST, US 6708305 B1

TITLE: Programmable array built-in self test method and controller with programmable expect generator, US 6553527 B1

TITLE: Reconfigurable built-in self-test engine for testing a reconfigurable memory, US 6769081 B1

TITLE: Programmable built-in self-test system for semiconductor memory device, US 6658611 B1

TITLE: Programmable built in self test for embedded DRAM, US 6415403 B1

TITLE: BIFEST: A Built-in Intermediate Fault effect sensing and test generation system for CMOS Bridging faults, author: Lee et al, ACM, April, 1999.

TITLE: Built-in Self-Test with an alternating Output, author: Bogue et al, IEEE, 1998.

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TITLE: Built-In Test Sequence Generation for Synchronous Sequential Circuits Based on Loading and Expansion of Test Subsequences, author: Pomeranz et al, ACM, 1999.

TITLE: Concurrent Test Scheduling in Built-In Self-Test environment, author: Chen et al, IEEE, 1992.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chameli Das whose telephone number is 571-272-2696.

The examiner can normally be reached on Monday-Friday from 7:00 A.M. to 3:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Tuan Dam can be reached at 571-272-2695. The fax number for this group is (703) 872-9306.

An inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is 571-272-2100.

*Chameli C. Das*  
**CHAMELI C. DAS**  
**PRIMARY EXAMINER**

*3/17/05*